Good memory Great company
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Practical Power-Related Issues

on Storage Solution for mobile device

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Contents

① Headaches

- ✓ Sudden Power Failure, Power On/Off
- ✓ Power Consumption, Power Budget
- ✓ Dynamic Power
- ✓ Static Power

② Serial IO vs. Static Power

- ✓ Power – PCIe/SATA
- ✓ Power – MIPI M-PHY

Sudden Power Failure, Power On/Off

❑ Sudden Power Failure(SPF)

- ✓ In case of SPF, **power-on slope**, fast or slow **power-off slope** can have an effect on NAND operation
- ✓ For instance, PMICs have normally LDO output discharge option for fast power-off slope
- ✓ **Power off notification** method using voltage detectors can help storage controllers mitigate the effect of SPF

❑ Normal Power On/Off

- ✓ The eMMC specification allows any order of power up of different power sources.
- ✓ NAND and controller should be designed to **avoid leakage current path** when both IO power and Core power are not supplied at the same time during power up.
- ✓ In sleep mode, the **unwanted leakage current path** can be occurred.

Power Consumption, Power Budget

❑ Power Estimation

- ✓ The power budget of PMICs are not always sufficient for latest storage solutions
- ✓ It is very usual for memory vendors to **estimate power consumption**
- ✓ **Peak power** is the most difficult to estimate and have the biggest relation with PMIC specification
- ✓ Power simulation using RC extraction considering practical FTL behavior is almost impossible to execute.
- ✓ Estimation using partially measured values such as single die operation or power simulation value using simplified FTL operation and so on

❑ Power Measurement

- ✓ Because of FTL, host requests do appear totally different behavior on NAND devices. It is **not easy to trigger the peak consumption point** to measure the peak power
- ✓ For PMICs do not supply sufficient power in general, memory vendors should provide power application guide to **reservoir peak power** for specific period of time.

Dynamic Power

- **The peak power consumption is more critical than RMS value to set makers**

- **NAND**
  - ✓ As the current NAND devices support **high speed interface and fast read/write**, a certain product needs much higher RMS power than legacy products for multi-way interleaving write.
  - ✓ In order to reduce peak power during interleaved write operation, **Peak Power Smoothing** can be considered

- **Controller**
  - ✓ Controllers are getting **faster and bigger** than ever.
  - ✓ The peak power consumption at controller side varies on each controller's SW and HW architecture.
  - ✓ A smart firmware logic can reduce peak power consumption depending on **HW/SW optimized storage controller**.
  - ✓ For RMS dynamic power, some vendors are utilizing power class.

Static Power

- **Current smart-phones require 1~3mA static power consumption for overall system.**

- **NAND**
  - ✓ STBY current of NAND devices are relatively small over that of controller

- **Controller**
  - ✓ Storage controllers normally use low-leakage library
  - ✓ For fast wake-up, certain amount of SRAM and glue logic should be powered at power saving mode
  - ✓ The leakage requirement to SRAM, logic, and analog IPs is tough very much
  - ✓ For instance, special design skills are needed to **wake-up fast(10's usec)** while consuming **low leakage current (< 100uA)**
    - Which can be one of the hurdles for SSD to penetrate mobile phone market

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Serial IO – PCIe/SATA

- **Even in the maximum power saving mode of SATA and PCIe, the static power consumption of a solution is around 10~20mW**
  - ✓ Because of squelch detect, Tx common mode keeper and leakage current

- **Serial IO PHY is the most dominant part of static power consumption**
  - ✓ **PHY – 50 ~ 60%**
  - ✓ Glue Logic, SRAM, etc – 20 ~ 30%
  - ✓ NAND Flash – 10 ~ 20%

- **One of the SATA PHYs has 6.5mW STBY mode current at slumber mode**

- **In order to try entering mobile device market, SSD makers are now trying to reduce static power consumption down to 5mW**
  - ✓ Generally speaking, less power means power-off more modules of PHY
  - ✓ Until now, **less static power** means **longer wake-up time**

Serial IO – PCIe/SATA

- **PCIe power saving efforts (L1 with CLKREQ)**
  - ✓ L1 wich CLKREQ
    - Turn off squelch detector and Root drive REFCLK to turn on end point's squelch
    - TxCommonMode, Leakage, REFCLK toggle detector are still consuming too much power(5~10mW)
  - ✓ L1.OFF(10uW) and L1.SNOOZ(100's uW)

- **SanDisk tried to add additional power saving mode**
  - ✓ PHYSLP, MEMSLP
  - ✓ More power saving means longer wake-up time

- **In mobile devices, less power and fast wake-up is the key success factor**

- **USFA seems to have learned the lesson…**

Serial IO – MIPI M-PHY

- **Less power means power-off more modules, especially power-guzzling blocks, such as PLL**
- **Turning off PLL means longer wake-up time because of PLL locking**
- **Using additional clock source, a UFS controller can respond to host while the PLL is locking up**
  - ✓ UFSA has two options, PWM and clock synchronous mode
  - ✓ It is said that UFS controller has 100's uW at STBY mode and almost same wake-up time with eMMC

Conclusion – from the power point of view

- Power has always been headaches of memory vendors which is getting worse as Flash technology evolves. Memory vendors have to have good understanding on mobile phones from the power point of view

- It is expected to see UFS adopted smart phones in the near future, however, no one knows if we can see SSD adopted mobile phones in the market.